REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official Action dated 23 February 2006. Responsive to the rejections made in the Official Action, Claims 12 and 19 have been amended to clarify the combination of elements which form the invention of the subject Patent Application. Claims 4 – 6, 8, 10 and 11 have been previously cancelled and acknowledgement of the allowance of Claims 1 – 3, 7, 9 and 16 – 18 is hereby made.

In the Official Action, the Examiner rejected Claim 12, 13, 14, and 19, and presumably Claim 20, under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Examiner stated that Claim 12 failed to point out the function of the interconnected elements. Accordingly, Claim 12 has been amended to clarify the claimed structure, adding the necessary functionality of the elements. Therefore, it is now believed that Claim 12 and the claims dependent thereon particularly point out and distinctly claim the subject matter that Applicant regards as the invention.

In the Official Action, the Examiner rejected Claims 12 – 14 and 19 under 35 U.S.C. § 102(e), as being anticipated by Sakaguchi, U.S. Patent No. 6,490,057.

Before discussing the reference relied upon by the Examiner, it is believed beneficial to first briefly review the structure of the invention of the subject Patent

Application, as now claimed. The invention of the subject Patent Application is directed to a device applied to scaling factor of horizontal scan of a scanner. The device includes an input operable to receive an input signal and at least an adder connected to the input. At least a shifter is provided that has an input terminal connected to the input for right shifting of the input signal, and an output terminal connected to an input of the adder for output of the right shifted input signal. The adder adds the right shifted input signal to the input signal to provide a combined signal to an output of the adder. The device includes an end shifter having an input terminal connected to the output of the adder and an output terminal connected to an output. The end shifter right shifts the combined signal to produce thereat an output signal that is a scaled reduction of the input signal.

In contradistinction, the Sakaguchi reference is directed to an image processing apparatus that enables an image read-out by a scanner to be enlarged with an arbitrary scale factor. In the embodiment of Fig. 4, a line memory is clocked utilizing a one-pixel pulse, or alternately the output of a thinned-out pulse generator 30. The selection of clock pulse is made through a clock change over switch, labeled 33 in Figure 4, but referred to by the reference number 81 in the Specification. The clock change over performs a switching function, connecting the terminals A and B selectively to the terminals a and b, the terminal a being coupled to the line memory 29 and the terminal b providing the output image transfer clock 24. Thus, in no way is the clock changeover an adder or equivalent

thereto and fails to add the right shifted input signal to the input signal to provide a combined signal to an output of the adder, as now claimed. In fact, one selection of the changeover connects the terminal A to a and B to b, column 9, lines 6 – 7, and in another configuration, connects terminal A to b and B to a, column 9, lines 16 – 17. Arguendo, even if one could consider the horizontal scanning thinned-out pulse generator 30 as being a shifter, the reference system does not include an end shifter having an input terminal connected at the output of the adder and an output terminal connected to an output, the end shifter right shifting the combined signal to produce thereat an output signal that is a scaled reduction of the input signal, as now claimed.

Further, with respect to Claim 19, nowhere does the reference disclose or suggest a plurality of series-connected adders and the at least a shifter including a plurality of shifters, each of the shifters providing a right shift of a respective input thereto, as now claimed. Still further, the reference fails to disclose or suggest each of the series-connected adders coupled at a first input thereof to an output of an adjacent one of the plurality of adders and coupled at a second input thereof to an output of a corresponding one of the plurality of adders for adding the output of the adjacent adder to the output of the corresponding shifter, as now claimed.

Additionally, again even if one could consider the horizontal scanning thinned-out pulse generator 30 as being a shifter, it is a one bit processing control circuit. Whereas, in the invention of the subject Patent Application the shifting

device is coupled to a multi-bit data path (e.g. 16 bits), providing a right-shift function.

Therefore, as the reference fails to disclose each and every one of the elements of the elements of Claims 12 and 19, it cannot anticipate those claims. Further, as the reference fails to suggest such a combination of elements, it cannot make obvious that invention either. Therefore, Claims 12 and 19, and the claims dependent thereon should now be allowable.

For all the foregoing reasons, it is now believed that the subject Patent Application has been placed in condition for allowance, and such action is respectfully requested.

Respectfully requested,
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